L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region, and

wherein said body portion includes a region extending from said body region in abutting relation with at least part of an outer periphery of said first and second semiconductor regions,

said MOS transistor further comprising

an isolation electrode formed on an insulating film formed on part of said body portion which is other than said body region and is in abutting relation with at least part of the outer periphery of said first and second semiconductor regions,

said at least one body contact including an out-of-isolation-electrode body contact formed on a region of said body portion which is opposed, as seen in plan view, to said first and second semiconductor regions with said isolation electrode therebetween.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-20 are pending in this application. Claims 17 and 20 have been withdrawn from consideration. Claims 6, 9, 11, 12, 16, and 19 have been amended to be rewritten in independent form without the introduction of any new matter.

The outstanding Action presents a rejection of Claims 1-5 and 18 as being obvious over Iwamatsu et al (the 1995 article entitled "*High-Speed 0.5μm SOI 1/8 Frequency Divider*

with Body-Fixed Structure for Wide Range of Applications) (Iwamatsu) in view of Agari[1] (JA 6-224302), Chen et al (U.S. Patent No. 5,767,549)(Chen), Blake et al (U.S. Patent No. 4,899,202, Blake), Gunning (U.S. Patent No.5,023,488), and Masuda et al (U.S. Patent No. 3,855,6109, Masuda). These outstanding rejections are traversed based upon the arguments presented in the last response that are incorporated herein by reference.

Applicants gratefully acknowledge the indication that Claims 6-16 and 19 would be allowed if rewritten to be in independent form so that Claim 6 would include all of the limitations of Claims 5, 3, and 1; Claim 9 would include al of the limitations of Claims 5, 3, and 1; Claim 11 would include al of the limitations of Claims 5, 3, and 1; Claim 12 would include al of the limitations of Claims 5, 3, and 1; Claim 16 would include al of the limitations of Claims 5, 3, and 1; and Claim 19 would include al of the limitations of Claims 18, 4, and 2.

As the present amendment rewrites Claims 6, 9, 11, 12, 16, and 19 in independent form so that Claim 6 includes all of the limitations of Claims 5, 3, and 1; Claim 9 includes all of the limitations of Claims 5, 3, and 1; Claim 11 includes all of the limitations of Claims 5, 3, and 1; Claim 12 includes all of the limitations of Claims 5, 3, and 1; Claim 16 includes all of the limitations of Claims 5, 3, and 1; and Claim 19 includes all of the limitations of Claims 18, 4, and 2, entry of the present amendment that adopts the Examiner's suggestion to place Claims 6, 9, 11, 12, 16, and 19 in independent form to secure the allowance thereof without the need for further search or other considerations is believed to be clearly in order.

Consequently, an early and favorable action indicating that Claims 6-16 and 19 are

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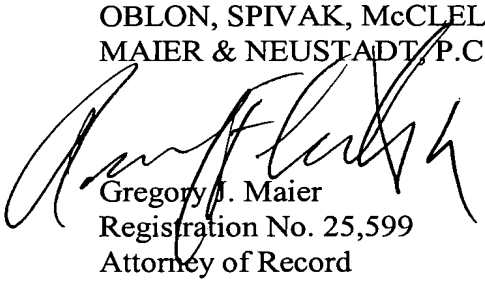
[1] Applicants assume that the indication of "Agair" on page 2 of the outstanding Action statement of the rejection instead of --Agari-- was a typographical error as no "Agair" reference is of record. Furthermore, as the response filed October 21, 2002 included no claim amendments, the present outstanding Action cannot be made final unless the previously relied upon --Agari-- reference was intended to be listed.

now formally allowed is earnestly and respectfully requested.

Furthermore, in light of the incorporated arguments from the previous response, it is believed that no other issues are outstanding in the present application that should now be considered to be in condition for formal allowance. Consequently, an early and favorable action to that effect is earnestly and respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Registration No. 25,599
Attorney of Record
Raymond F. Cardillo, Jr.
Registration No. 40,440

22850

(703) 413-3000
Fax #: (703) 413-2220

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Amendment Filed: 6-16-03

6. (Amended) [The] A semiconductor device [according to Claim 5] including an MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer, said MOS transistor being operated based on a predetermined clock,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said MOS transistor being formed by a method comprising the steps of:

(a) providing an operating frequency of said predetermined clock; and

(b) determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$R \cdot C \cdot f < 1$

where

C = the gate capacitance said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

f = the operating frequency of said predetermined clock, and

$f \geq 500$ MHZ,

wherein said resistance R of said fixed potential transmission path is determined by

$R = (\rho \cdot W)/(L \cdot t_{SOI})$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region, and

wherein said body portion includes a region extending from said body region in abutting relation with at least part of an outer periphery of said first and second semiconductor regions,

said MOS transistor further comprising

an isolation electrode formed on an insulating film formed on part of said body portion which is other than said body region and is in abutting relation with at least part of the outer periphery of said first and second semiconductor regions,

said at least one body contact including an out-of-isolation-electrode body contact

formed on a region of said body portion which is opposed, as seen in plan view, to said first and second semiconductor regions with said isolation electrode therebetween.

9. (Amended) [The] A semiconductor device [according to Claim 5] including an MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer, said MOS transistor being operated based on a predetermined clock,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said MOS transistor being formed by a method comprising the steps of:

(a) providing an operating frequency of said predetermined clock; and

(b) determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$$R \cdot C \cdot f \leq 1$$

where

C = the gate capacitance said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

f = the operating frequency of said predetermined clock, and

$f \geq 500$ MHZ

wherein said resistance R of said fixed potential transmission path is determined by

$R = (\rho \cdot W)/(L \cdot t_{SOI})$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region,

wherein said body portion includes a region disposed in abutting relation with said first and second semiconductor regions along the gate width and extending from said body region along the gate length,

wherein said gate electrode is formed on part of said body portion which is disposed in abutting relation with said first and second semiconductor regions along the gate width, and extends further from on said body region along said gate length, and

wherein said at least one body contact includes an out-of-gate-electrode body contact from on said region of said body portion which is opposed, as seen in plan view, to said first and second semiconductor regions, with said gate electrode therebetween.

11. (Amended) [The] A semiconductor device [according to Claim 5] including an

MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer, said MOS transistor being operated based on a predetermined clock,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said MOS transistor being formed by a method comprising the steps of:

(a) providing an operating frequency of said predetermined clock; and

(b) determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$$R \cdot C \cdot f \leq 1$$

where

C = the gate capacitance said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

f = the operating frequency of said predetermined clock, and

$f \geq 500$ MHZ,

wherein said resistance R of said fixed potential transmission path is determined by

$R = (\rho \cdot W)/(L \cdot t_{SOI})$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region, and

wherein said at least one body contact includes:

a first body contact formed on said body portion in a position located on an outward extension line from one end of said gate electrode along the gate width, and

a second body contact formed on said body portion in a position located on an outward extension linen from the other end of said gate electrode along the gate width.

12. (Amended) [The] A semiconductor device [according to Claim 5] including an MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer, said MOS transistor being operated based on a predetermined clock,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said MOS transistor being formed by a method comprising the steps of:

(a) providing an operating frequency of said predetermined clock; and

(b) determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$$R \cdot C \cdot f < 1$$

where

C = the gate capacitance said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

f = the operating frequency of said predetermined clock, and

$f \geq 500$ MHZ,

wherein said resistance R of said fixed potential transmission path is determined by

$$R = (\rho \cdot W)/(L \cdot t_{SOI})$$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region, and

wherein said body region includes a first body region at least part of which is formed in an upper part thereof, and a second body region formed in a lower part thereof,

said second body region of the second conductivity type being of an impurity concentration higher than the impurity concentration of said first body region of the second conductivity type.

16. (Amended) [The] A semiconductor device [according to Claim 5] including an MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer, said MOS transistor being operated based on a predetermined clock,

the semiconductor device further comprising:

a body floating MOS transistor having an unfixed body potential,

said SOI layer including a first region of a first conductivity type having a first thickness, and a second region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region having a second thickness less than said first thickness,

said MOS transistor being formed on said first region,

said body floating MOS transistor being formed on said second region,

said MOS transistor comprising,

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions,

a gate electrode formed on a gate oxide film formed on said body region, and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said MOS transistor being formed by a method comprising the steps of:

(a) providing an operating frequency of said predetermined clock; and

(b) determining a layout pattern of said MOS transistor based on the operating frequency of said predetermined clock,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$$R \cdot C \cdot f \leq 1$$

where

C = the gate capacitance said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

f = the operating frequency of said predetermined clock, and

$f \geq 500$ MHZ,

wherein said resistance R of said fixed potential transmission path is determined by

$$R = (\rho \cdot W)/(L \cdot t_{SOI})$$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the

gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region.

19. (Amended) [The] A semiconductor device [according to Claim 18] including an MOS transistor formed on an SOI substrate including a supporting substrate, a buried oxide film and an SOI layer,

said MOS transistor comprising:

a first semiconductor region of a first conductivity type and selectively formed in said SOI layer;

a second semiconductor region of said first conductivity type and selectively formed in said SOI layer independently of said first semiconductor region;

a body portion of a second conductivity type and including a body region, said body region being a region of said SOI layer which lies between said first and second semiconductor regions;

a gate electrode formed on a gate oxide film formed on said body region, said gate electrode being electrically connected to said body portion; and

at least one body contact electrically connected to said body portion and receiving a fixed potential,

said MOS transistor being formed by a method comprising the steps of:

(a) providing a signal propagation delay time required for said MOS transistor; and

(b) determining a layout pattern of said MOS transistor based on said signal propagation delay time,

wherein the layout pattern of said MOS transistor is determined in said step (b) so as to satisfy the conditional expression

$(R \cdot C)/td < 1$

where

C = the gate capacitance of said MOS transistor,

R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region,

td = signal propagation delay time (s) required for said MOS transistor, and

$td \leq 50$ ps,

wherein said resistance R of said fixed potential transmission path is a determined by

$R = (\rho \cdot W)/(L\text{-}t_{SOI})$

where

W = the length of said fixed potential transmission path in said body region along the gate width of said gate electrode,

L = the length of said fixed potential transmission path in said body region along the gate length of said gate electrode,

t_{SOI} = the thickness of said SOI layer, and

ρ = the resistivity of said body region, and

wherein said body portion includes a region extending from said body region in abutting relation with at least part of an outer periphery of said first and second semiconductor regions,

said MOS transistor further comprising

an isolation electrode formed on an insulating film formed on part of said body portion which is other than said body region and is in abutting relation with at least part of the outer periphery of said first and second semiconductor regions,

said at least one body contact including an out-of-isolation-electrode body contact

formed on a region of said body portion which is opposed, as seen in plan view, to said first and second semiconductor regions with said isolation electrode therebetween.